I·2₁

06ELN15/25

USN | | | | | | | | | | |

NEW SCHEME

SRINIVAS INSTITUTE OF TECHNOLOGY
LIBRARY, MANGALORE

# First / Second Semester B.E. Degree Examination, Dec.06 / Jan.07
## Common to all Branches
## Basic Electronics

Time: 3 hrs.] [Max. Marks:100

**Note:** ***1. Answer any FIVE questions selecting at least two questions from each part***

## Part A

1 a. Explain the operation of a half-wave rectifier with capacitor filter with the help of a circuit diagram and relevant waveforms. **(08 Marks)**

b. With a neat circuit diagram, explain Zener diode voltage regulator. **(06 Marks)**

c. A full-wave bridge rectifier supplies a load of 400 Ω in parallel with a capacitor of 500 μF. If the ac supply voltage is $230\sin 314t$ V, find the

i) Ripple factor and

ii) DC load current. **(06 Marks)**

2 a. Draw the input and output characteristics curve of a transistor in common-emitter configuration. Explain their nature and shape. What do their slope represent? **(07 Marks)**

b. What are the different current components in the three regions of a transistor when it is functioning in active region? Depict them in suitable diagrams giving their origin. **(06 Marks)**

c. For the circuit shown below, the parameters are $V_{BB} = 1.5$ V, $R_B = 580$ kΩ, $V_{CC} = 5$ V, $V_{EB}$ (on) = 0.6 V and $\beta = 100$. Find $I_B$, $I_C$, $I_E$ and $R_C$ such that $V_{EC} = \frac{1}{2}(V_{CC})$. **(07 Marks)**

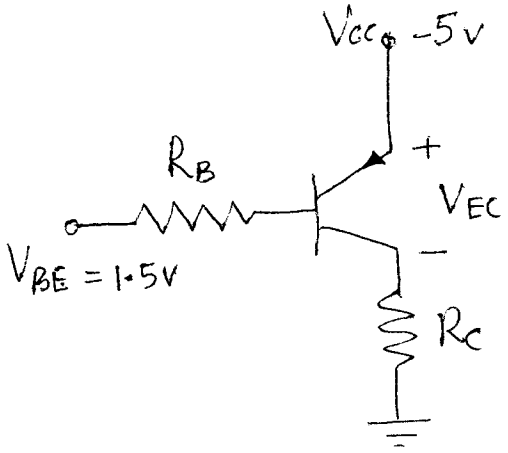



Fig. Q2 (c)

3 a. What is a DC load line? **(02 Marks)**

b. List the different biasing circuits and explain collector-base bias circuit. **(10 Marks)**

c. For the base bias circuit for a npn transistor find $I_B$, $I_C$ and $V_{CE}$, if $R_C = 2.2$ kΩ, $R_B = 470$ kΩ, $V_{CC} = 18$ V, $h_{FE} = 100$, $V_{BE} = 0.7$ V. Draw the DC load line and indicate the Q point. **(08 Marks)**

*Contd....2*

I·2₂
Srinivas Institute of Technology
Library, Mangalore



4 a. With respect to SCR, define the following :
   i) Holding current $I_H$.
   ii) Gate trigger voltage $V_{GT}$.
   iii) Peak forward voltage $V_{DRM}$.
   iv) Maximum RMS current $I_T$(rms). **(06 Marks)**

b. Sketch the typical UJT emitter characteristics for $I_{B_2} = 0$, $V_{B_1}V_{B_2} = 20$ V and $V_{B_1}V_{B_2} = 5$ V. Identify each region and important points on the characteristics. **(06 Marks)**

c. Draw the complete equivalent circuit of a JFET. Explain each component. **(08 Marks)**

## Part B

5 a. Compare positive feedback amplifier with negative feedback amplifier with the help of a neat block diagram. **(12 Marks)**

b. Calculate the frequency of oscillations of the Hartley Oscillator which has $L_1 = 0.5$ mH, $L_2 = 1$mH and $C = 0.2\ \mu F$. What should be the value of C, if the frequency of oscillation were to be 12 kHz with other components of the circuit intact? **(08 Marks)**

6 a. Describe an Op-Amp and its important characteristics. **(06 Marks)**

b. What is saturating property of an Op-Amp? Mention the typical value if saturating output voltage for an IC-741 Op-Amp operating at ± 12 V DC supply. **(06 Marks)**

c. With a neat diagram explain the internal structure of a cathode ray oscilloscope. Explain the different sections and the various electrodes. **(08 Marks)**

7 a. Convert $(3576)_8$ to hexadecimal. **(05 Marks)**

b. Convert $(725.25)_8$ to its decimal and binary equivalent. **(05 Marks)**

c. Subtract $(111001)_2$ from $(101011)_2$ using 2's compliment method. **(05 Marks)**

d. For an AM, amplitude of modulating signal is 0.5 V and carrier amplitude is 1 V. Find modulation index. **(05 Marks)**

8 a. Realize AND gate using diodes. **(05 Marks)**

b. Implement XNOR using only NOR gate. **(05 Marks)**

c. List the properties of Boolean Algebra with an example. **(05 Marks)**

d. Prove that $\overline{\overline{AB} + \overline{A} + AB} = 0$. **(05 Marks)**

*****

Srinivas Institute of Technology
Library, Mangalore



06ELN15/25

USN | | | | | | | | | | |

# First/Second Semester B.E. Degree Examination, July 2007
## Common to All Branches
## Basic Electronics

SRINIVAS INSTITUTE OF TECHNOLOGY
LIBRARY, MANGALORE

Time: 3 hrs.] [Max. Marks:100

**Note : *Answer any FIVE full questions selecting at least TWO questions from each part.***

### PART - A

1 a. Define reverse recovery time in a diode. How is the reverse recovery time kept minimal? **(05 Marks)**

b. Define ripple factor. Find the ripple factor of a half wave rectifier. **(06 Marks)**

c. In a full wave rectifier, the input is from a 30 – 0 – 30V transformer. The load and diode forward resistances are 100Ω and 10Ω respectively. Calculate the average voltage, rectification efficiency and percentage regulation. **(05 Marks)**

d. What is a voltage regulator? Why is it necessary? **(04 Marks)**

2 a. What are the biasing conditions required to make a transistor to act as current amplifier. Explain the reason for the same. **(07 Marks)**

b. Why the collector – base junction can be thought of as a leaky diode in a CE configuration? Describe the current components in the three regions of a transistor when it is functioning in the active region. Depict them with suitable diagrams giving their origin. **(08 Marks)**

c. For the transistor in Fig.2(c), $\beta = 30$, determine $V_1$ such that $V_{CEQ} = 6V$. **(05 Marks)**

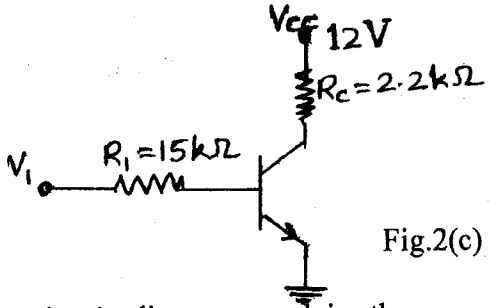



Fig.2(c)

Assume $V_{BE}$ suitably.

3 a. With a circuit diagram, explain the operation of collector to base bias circuit. Explain how this circuit significantly improves the bias stability for $h_{FE}$ changes compared to base bias. **(10 Marks)**

b. A collector to base bias circuit has $V_{CC} = 5V$, $R_C = 5.6\,k\Omega$, $R_B = 82\,k\Omega$ and $V_{CE} = 5V$. Determine the transistor $h_{FE}$ value. Calculate new $V_{CE}$ level when a transistor with $h_{FE} = 50$ is substituted. **(10 Marks)**

4 a. Explain the construction and working of SCR. Give the two transistor equivalent circuit and label all the terminals. **(08 Marks)**

b. Explain the basic construction and operation of UJT. Draw the equivalent circuit of UJT. **(08 Marks)**

c. With respect to JFET define the following. i) pinch off coltage ($V_P$) ii) Saturation drain current $I_{DSS}$. **(04 Marks)**

*Contd...2*

Srinivas Institute of Technology
Library, Mangalore


## PART – B

5 a. Estimate the values of R and C for an output frequency of 1kHz in a RC phase shift oscillator. Assume $R_C = 4k\Omega$, $V_{CC} = 12V$, $\beta = 75$. **(06 Marks)**

b. Explain with neat block diagram Barkhausen criterion to generate oscillations, with special reference to the condition $A\beta < 1$, $A\beta > 1$, $A\beta = 1$. **(08 Marks)**

c. The gain of a transistor amplifier is 40. If positive feedback is introduced with $\beta = 0.025$, estimate the gain of the amplifier with feedback. Also estimate the gain of the amplifier if negative feedback is introduced with $\beta = 0.025$. **(04 Marks)**

6 a. Explain why closed loop configuration of op amp is used in all the practical amplifier circuit and bring out the advantages of closed loop operation with negative feedback. **(06 Marks)**

b. Draw the non inverting voltage amplifier circuit using an op amp and show that the closed loop voltage gain is given by $A_{V_f} = \frac{A_v}{(1 + A_v\beta)}$.

Where $A_v$ = open loop voltage gain of an op amp.

$\beta$ = feedback factor. **(06 Marks)**

c. An inverting amplifier circuit has input series resistor of $20k\Omega$, feedback resistor of $100k\Omega$ and a load resistor of $50k\Omega$. Draw the circuit and calculate the input current, load current, and the output voltage when the applied input voltage is equal to +1.5V. **(08 Marks)**

7 a. Calculate modulation index using AM wave. **(05 Marks)**

b. Convert each decimal to binary i) 11.125 ii) 0.625 **(05 Marks)**

c. Determine the base value of x if $(211)_x = (152)_8$. **(05 Marks)**

d. A carrier of 500 W, 1MHz, is amplitude modulated with sinusoidal signal of 1kHz, depth of modulation is 60%. Calculate bandwidth, power in the sidebands and total power transmitted. **(05 Marks)**

8 a. Write the boolean expression for output Y, for the following logic circuit: **(05 Marks)**

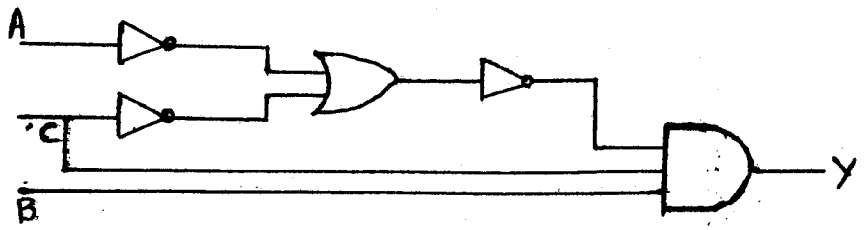



Fig.8(a)

b. Realise following expression using NOR gates $Y = A(\overline{B} + C)$. **(05 Marks)**

c. Simplify using DeMorgan's theorem.

$\overline{ABCD}$ **(05 Marks)**

d. Realise full adder using two half adders and OR gate. **(05 Marks)**

*****

Srinivas Institute of Technology
Library, Mangalore

USN | | | | | | | | | | |

06ELN15/25

# First/Second Semester B.E. Degree Examination, June / July 08

## Basic Electronics

Time: 3 hrs. Max. Marks:100

**Note :** ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

### PART - A

1 a. Sketch typical V – I characteristics of a pn junction. Explain the shape of the V – I characteristics and identify the important points. **(06 Marks)**

b. Draw the circuit of a full wave Bridge Rectifier and show that ripple factor = 0.48 and efficiency = 81%. **(06 Marks)**

c. Design a Zener Regulator with the following specifications.
$V_O$ = 12 V, Vin = (25 to 35)V, $I_L$ = (35 to 55)mA and $I_Z$ = (25 to 45)mA. **(08 Marks)**

2 a. Show that a transistor can be used as an amplifier. **(06 Marks)**

b. Sketch the typical input and output characteristics of an NPN transistor and explain the three regions of operation. **(08 Marks)**

c. Calculate $\alpha_{dc}$ and $\beta_{dc}$ for the transistor if Ic is measured as 1mA and $I_B$ is 25 μA. Also determine the new base current to give Ic = 5 mA. **(06 Marks)**

3 a. Define biasing of a transistor. Compare the base bias, collector to base bias and voltage divider bias and discuss the advantages and disadvantages of the three types of bias circuits. **(10 Marks)**

b. Design the voltage divider bias circuit as shown in Fig. Q 3(b).

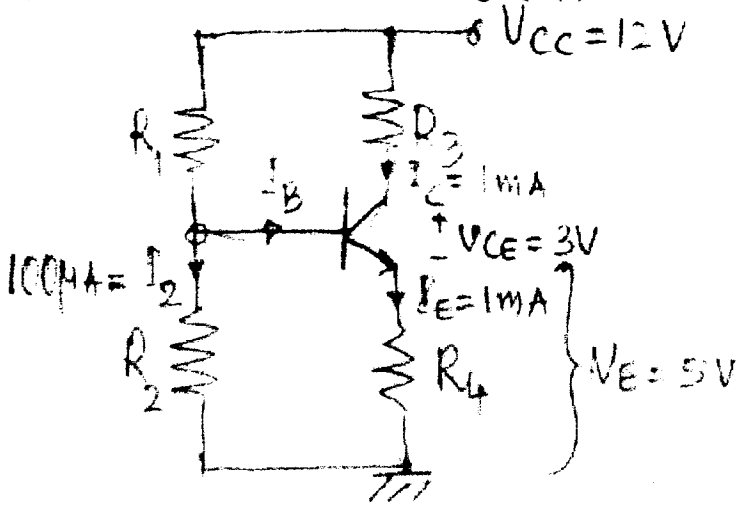



Fig. Q 3(b)

The bias conditions are to be $V_{CE}$ = 3 V, $V_E$ = 5 V and Ic = 1 mA. **(10 Marks)**

4 a. Sketch a block diagram to represent an n – channel FET. Indicate voltage and current direction and the device operation. **(06 Marks)**

b. Draw sketches to show the basic construction and equivalent circuit of a UJT. Briefly explain the device operation. **(06 Marks)**

c. Draw the diagram of an SCR Zero Point triggering circuit. Explain the circuit operation and advantages and draw the load wave form. **(08 Marks)**

II 3₂

Srinivas Institute of Technology
Library, Mangalore

## PART – B

5 a. Sketch the circuit of a two page capacitor coupled, CE amplifier, and e

b. Explain the Barkhausen criterion for oscillation.

c. In a Colpitt's Oscillator, if the desired frequency is 800 kHz, determine C.

6 a. Mention the ideal characteristics of an OP – AMP.

b. Explain the working of a CRT.

c. Design a scaling adder circuit using an OP – AMP to give the outp
$V_O = -(3V_1 + 4V_2 + 5V_3)$, given the inputs $V_1$, $V_2$, $V_3$.

7 a. Explain the need for modulation.

b. Draw the block diagram of a super heterodyne AM receiver and exp each block.

c. Solve :

i) $[0.7642]_{10} = [?]_2$

ii) $[AD6CB]_{16} = [?]_8$

iii) $[11011.1011]_2 = [?]_8$

iv) Substract using 2's complement, 66 – 64

v) Add $[24]_8$ to $[66]_8$

vi) $[1011.11001]_2 = [?]_{10}$.

8 a. i) Prove that
$AB + A + AB = 0$

ii) Simplify
$\overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y} + X\overline{Y}$.

b. Draw the logic circuit for Full Adder and write its truth table with expr

c. Explain how AND, OR and NOT gates can be obtained using only NA

*****

Srinivas Institute of Technology
Library, Mangalore

USN | | | | | | | | | | |

06ELN15/25

# First / Second Semester B.E. Degree Examination, Dec. 07 / Jan. 08
## Basic Electronics

Time: 3 hrs. Max. Marks:100

**Note :** ***Answer any FIVE full questions selecting at least two questions from each part.***

### Part A

1 a. Define DC load line for a diode and explain the DC load line for circuit consisting of supply voltage in series with resistance and diode. **(06 Marks)**

b. Draw the circuit of a bridge rectifier and show that ripple factor of a bridge rectifier is 0.48. **(08 Marks)**

c. Explain how Zener diode can be used as voltage regulator. **(06 Marks)**

2 a. Draw a sketch to show the various current components in a NPN transistor and deduce the relation between various current components. **(08 Marks)**

b. Sketch typical transistor input and output characteristics for CE configuration and briefly explain the three regions of operation. **(07 Marks)**

c. For the circuit shown in figure Q2 (c). Compute i) Three transistor currents ii) Voltage drop across $R_C$ & $R_B$. **(05 Marks)**

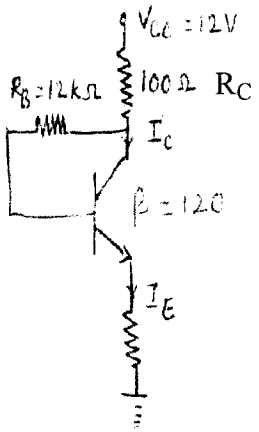



Fig. Q2 (c)

3 a. Define Biasing of Transistor. Explain with neat circuit the operation of voltage divider bias circuit. **(06 Marks)**

b. Transistor is biased in voltage divider bias circuit with $R_1 = 47K\Omega$, $R_2 = 15K\Omega$, $R_C = 1.5K\Omega$, $R_E = 1K\Omega$, $V_{CC} = 15V$. Compute emitter voltage ($V_E$), Collector voltage ($V_C$) and Collector to emitter voltage ($V_{CE}$). **(08 Marks)**

c. Discuss the thermal stability of transistor bias circuit with respect to $I_{CBO}$ and $V_{BE}$. **(06 Marks)**

4 a. With neat circuit diagram and waveform, explain how SCR can be triggered by application of pulse at Gate. **(06 Marks)**

b. Define the following with respect to UJT:
i) Interbase resistance.
ii) Valley point current.
iii) Negative resistance region. **(06 Marks)**

c. A typical JFET amplifier is shown in figure Q4 (c). Calculate the maximum and minimum output voltage produced by a ± 30 mV ac input and also calculate the circuit voltage gain in each case given forward transfer admittance ($Y_{fs(max)}$ = 5000 µs, $Y_{fs(min)}$ = 1000 µs). **(08 Marks)**

I.3₂
Srinivas Institute of Technology
Library, Mangalore



4 c.

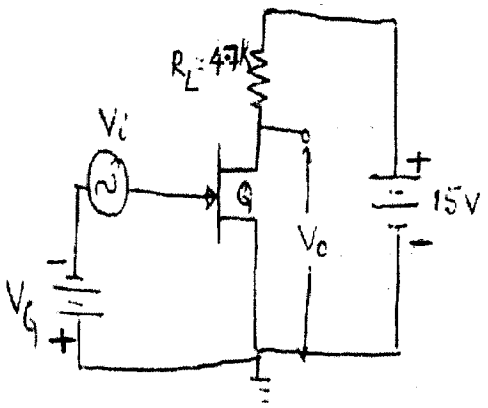



Fig. Q4 (c)

**Part B**

5 a. With neat circuit diagram and frequency response, explain the operation of single stage RC coupled amplifier. **(06 Marks)**

b. Obtain an equation for overall voltage gain with negative feed back of negative feed back amplifier. **(06 Marks)**

c. Calculate the frequency of oscillations of Colpitt's oscillator having $C_1 = 2000$ pF, $C_2 = 1000$ pF and $L = 4$ mH. What should be the value of L if the frequency of oscillation is 140 KHz. **(08 Marks)**

6 a. Draw the circuit of op-amp as integrator and derive an expression for output voltage. **(06 Marks)**

b. A non inverting amplifier has input resistance 10 KΩ and feed back resistance 60 KΩ with load resistance 47 KΩ. Draw the circuit and calculate output voltage, voltage gain and load current when input voltage is 1.5 V. **(08 Marks)**

c. List the ideal characteristics of an op-amp. **(06 Marks)**

7 a. Draw the block diagram of a super heterodyne AM receiver and explain the functions of each block. **(10 Marks)**

b. A carrier of 750 W, 1 MHz is amplitude modulated by sinusoidal signal of 2 KHz to a depth of 50% calculate Band width Power in side band and total power transmitted. **(06 Marks)**

c. Convert the following hexadecimal number into decimal.
i) A3BH
ii) 2F3H **(04 Marks)**

8 a. Realize the following expression using Basic gates:
i) $Y = \overline{B}\,\overline{C} + \overline{A}\,\overline{C} + \overline{A}\,\overline{B}$.
ii) $Y = A\overline{B} + \overline{A}B$
iii) $Y = \overline{AB} + A + \overline{(B+C)}$ **(06 Marks)**

b. Simplify the following Boolean Expressions
i) $AB + \overline{AC} + A\overline{B}C(AB + C)$.
ii) $\overline{\overline{A\overline{B}} + ABC + A(B + A\overline{B})}$ **(06 Marks)**

c. Realize Full adder circuit using NAND gate and write its truth table. **(08 Marks)**

*****

Srinivas Institute of Technology
Library, Mangalore

USN | | | | | | | | | | |

06ELN15/25

# First / Second Semester B.E. Degree Examination, Dec 08 / Jan 09
## Basic Electronics

Time: 3 hrs. Max. Marks:100

**Note :** *1. Answer any FIVE full questions, selecting atleast two questions from each Part.*
*2. Answer all objective type questions only in first and second writing pages.*
*3. Answer for objective type questions shall not be repeated.*

### PART – A

1 a. i) The Knee voltage of a silicon diode is _____ volts.
A) 0.3V B) 0.5V C) 0.7V D) None of these
ii) The depletion layer capacitance effect occurs in a diode when it is _____
A) Forward biased B) Reverse biased C) Unbiased D) All of these
iii) The efficiency of full wave rectifier is about _____%.
A) 40.6 B) 0.46 C) 1.21 D) 81.2
iv) Zenor diode used as a voltage regulator when it is _____ biased.
A) Forward B) Reverse C) Unbiased D) none of these. **(04 Marks)**

b. What is a PN Junction? Draw and explain the V – I characteristics of PN Junction. **(08 Marks)**

c. Derive an expression for ripple factor and output DC voltage of a full wave rectifier with C filter. **(08 Marks)**

2 a. i) In the saturation region, the Collector - base and Emitter – base Junctions are _____ biased.
A) Forward B) Reverse C) Unbiased D) none of these
ii) Common - emitter current gain (Bdc) of a transistor is given by_____
A) $\frac{I_C}{I_B}$ B) $\frac{I_E}{I_C}$ C) $\frac{I_C}{I_E}$ D) none of these
iii) In a transistor the current conduction is due to _____ carriers.
A) Majority B) Minority C) Both D) none of these.
iv) The stability factor 'S' is the rate of change of collector current with respect to _____.
A) Reverse saturation current B) Collector current
C) Emitter current D) Base current. **(04 Marks)**

b. Draw input and output characteristics of a transistor in common base configuration and explain in detail. **(08 Marks)**

c. Obtain the relationship between Ldc and Bdc. **(04 Marks)**

d. Calculate the values of $I_C$, $I_E$ and Bdc for a transistor with Ldc = 0.98 and $I_B$ = 120 μA. **(04 Marks)**

3 a. i) The intersection of DC load line and the output characteristics of a transistor is called _____
A) Q – Point B) Quiescent Point C) Operating Point D) All of these.
ii) The biasing circuit, which gives most stable operating point is _____
A) Base Bias B) Collector to Base Bias
C) Voltage divider Bias D) None of these.

iii) Reverse saturation current doubles for every _____ $^0$C rise in temperature
A) 50 B) 40 C) 30 D) 10

iv) Reverse recovery time can be kept minimum with the following condition_____
A) $t_{f(min)} = 10$ trr B) $t_{f(min)} = 0.1$ trr C) $t_{f(max)} = $ trr D) none of these
**(04 Marks)**

b. List the transistor biasing circuits. Explain with neat circuit the operation of Base bias. **(08 Marks)**

c. Design a collector – to - Base bias circuit to have $V_{CE} = 5V$ and $I_C = 5mA$, When the supply voltage is 15V and Bdc = 100, assume silicon transistor. **(08 Marks)**

4 a. i) SCR can be analyzed using_____
A) Two transistor B) Three transistor C) Four transistor D) All the above.

ii) FET is a_____ controlled device.
A) Voltage B) Current C) Power D) none of these

iii) In UJT the region of the characteristics between peak point and valley point is called _____ region.
A) Negative resistance B) Positive resistance C) Active D) All the above

iv) Latching current in SCR is _____than holding current.
A) more B) less C) equal D) none of these **(04 Marks)**

b. Explain the operation of SCR using the two transistor equivalent circuit. **(08 Marks)**

c. Explain the basic construction and equivalent circuit of UJT. **(08 Marks)**

## PART – B

5 a. i) Oscillator uses_____ type of feedback.
A) Positive B) Negative C) Reverse D) None of these.

ii) Negative feedback results in_____ Bandwidth.
A) Increased B) Decreased C) Zero D) None

iii) The frequency of Hantley Oscillator is given by f = _____
A) $\frac{1}{2\pi\sqrt{LC}}$ B) $\frac{1}{2\pi\sqrt{RC}}$ C) $\frac{1}{2\pi\sqrt{C}}$ D) $\frac{1}{2\pi LC}$

iv) The overall voltage gain of two stage capacitor coupled CE amplifier is _____ than a single stage CE amplifier.
A) greater B) less C) equal D) none **(04 Marks)**

b. With a neat circuit diagram and frequency response, explain the operation of single stage common – emitter amplifier. **(08 Marks)**

c. Draw the circuit of transistor RC phase shift oscillator and explain the significance of each component. **(08 Marks)**

6 a. i) Common mode rejection ratio of ideal Op AMP is _____.
A) 0 B) 90 C) $\infty$ D) 180.

ii) The gain of voltage follower is_____
A) Unity B) Zero C) $\infty$ D) None.

iii) In inverting amplifier there is _____ phase shift with input and output.
A) $0^0$ B) $90^0$ C) $180^0$ D) $360^0$.

iv) The maximum rate at which amplifier output can change in volts per microsecond (V/μs) is called_____
A) Over rate B) Slew rate C) Under rate D) None **(04 Marks)**

b. Draw the block diagram of CRO and explain the function of each stage. **(08 Marks)**

Srinivas Institute of Technology
Library, Mangalore



c. Calculate the output voltage of the following circuit given below **(08 Marks)**

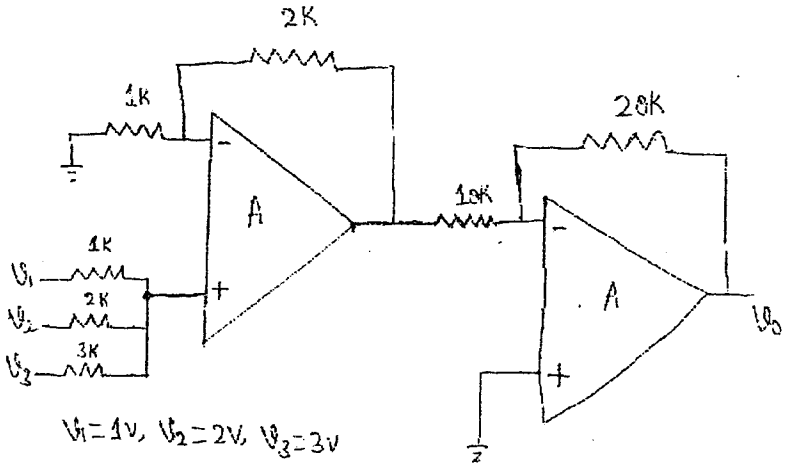



Fig. Q6(c).

7 a. i) $(25)_{10} = (\ ?\ )_2$.
A) $(00111)_2$ B) $(11001)_2$ C) $(11000)_2$ D) $(00011)_2$.

ii) $(101011.11001)_2 = (\ ?\ )_{16}$.
A) $(AB.2C)_{16}$ B) $(2C.B8)_{16}$ C) $(2B.C8)_{16}$ D) $(2C.2D)_{16}$.

iii) $\overline{2}$'S of binary number 10110 is_____
A) 00011 B) 01010 C) 11100 D) 11111

iv) $(763.634)_8 = (\ ?\ )_2$.
A) $(111110011.110011100)_2$ B) $(101011001.110011001)_2$.
C) $(000011110.111100001)_2$ D) $(010101010.001100110)_2$. **(04 Marks)**

b. Subtract using 2's complement.
i) [ 4 – 9 ] ii) [ 8 – 2 ]. **(04 Marks)**

c. Explain the need of modulation. **(04 Marks)**

d. Draw the block diagram of a superheterodyne receiver and explain the function of each block. **(08 Marks)**

8 a. i) Demorgan theorem states that $\overline{A+B}$ = _____
A) $\overline{A}+\overline{B}$ B) $\overline{A}\ .\ \overline{B}$ C) $\overline{AB}$ D) None.

ii) Universal gates are_____ and _____
A) NOT and NOR B) AND and OR
C) NAND and NOR D) EXOR and EX-NOR

iii) $A + AB + A$ = _____
A) AB B) $A+B$ C) A D) O.

iv) The output is High when all the outputs are high, such a gate is called.
A) NAND B) NOR C) AND D) OR **(04 Marks)**

b. Simplify the following Boolean expressions
i) $y = \overline{\overline{AB}+\overline{A}+AB}$ ii) $y = AB + A(B + C) + B(B + C)$. **(06 Marks)**

c. Realize the following expressions using only NAND gates.
i) $y = a\overline{b} + \overline{a}b$ ii) $y = (A + \overline{B} + C).(\overline{A} + B + C)$ **(06 Marks)**

d. Realize a full adder using two half adders. **(04 Marks)**

*****

USN | | | | | | | | | | |

06ELN15/25

# First / Second Semester B.E. Degree Examination, June-July 2009
## Basic Electronics

Time: 3 hrs. Max. Marks:100

**Note : 1.** ***Answer any Five full question, choosing at least two from each part.***
**2.** ***Answer all objectives type questions only in OMR sheet page 5 of the Answer Booklet.***
**3.** ***Answer to the objective type questions on sheets other than OMR will not be valued***

## PART – A

1 a. i) Zener diode acts as a _____ device.
A) Constant current B) Constant voltage
C) Constant power D) Variable voltage.

ii) The barrier potential of a silicon p-n junction is approximately
A) 0.3 V B) 0.1 V C) 0.7 V D) 1.2 V.

iii) In reverse bias the diode can be represented as
A) Open circuit B) Short circuit
C) A battery of 0.7 V D) A current source with constant current.

iv) A half wave rectifier is fed from secondary of a transformer whose output voltage is 12.6 V. The DC voltage of the rectifier output is
A) 12.6 V B) 5.66 V C) 17.8 V D) 11.32 V **(04 Marks)**

b. Draw a full wave rectifier and give the expressions for i) DC voltage; ii) Ripple frequency; iii) PIV; iv) Efficiency; v) RMS value of voltage. What are its advantages over half-wave rectifier? **(08 Marks)**

c. A Zener diode has a breakdown voltage of 10 V. It is supplied from a voltage source varying between 20-40 V in series with a resistance of 820 Ω. Using an ideal Zener model obtain the minimum and maximum Zener currents. **(08 Marks)**

2 a. i) In a transistor the part heavily doped is
A) Emitter B) Base C) Collector D) All are equally doped

ii) The relation between α and β is given by
A) $\alpha = \beta$ B) $\alpha = \frac{\beta}{1-\beta}$ C) $\alpha = \frac{\beta}{1+\beta}$ D) $\alpha = \frac{1}{\beta}$

iii) In the active region the collector – Base junction is
A) Forward biased B) Reverse biased
C) Driven from Forward bias to reverse bias D) Not biased

iv) In CE configuration, when collector current is zero, VCE equals
A) $\frac{V_{CC}}{R_C + R_E}$ B) $V_{CC}$ C) $\frac{V_{CC}}{R_C}$ D) $\frac{V_{CC}}{R_E}$ **(04 Marks)**

b. Draw the common Emitter circuit. Draw the input and output curves and explain the terms active region, cut off region and saturation region. **(08 Marks)**

c. Determine the transistor currents in the Fig.Q.2(c) if β = 100 **(08 Marks)**

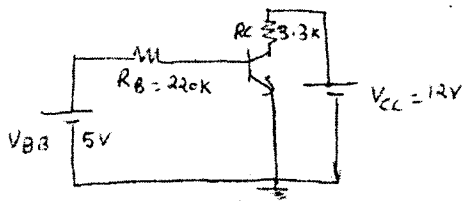



Fig.Q.2(c).

3 a. i) When used as a switch the transistor operates in
A) Active region B) Saturation and cut off C) Cut off region D) Active and saturation.

ii) When used as an amplifier the transistor operates in
A) Active region B) Saturation region C) Cut off region D) Can be in any of them

iii) Even with sinusoidal base current we get non-sinusoidal collector current in common emitter configuration because of
A) Noise introduced in base current B) Large resistance of signal source
C) Large input resistance of transistor D) Non parallel output characteristics

iv) The stability factor S is the rate of change of collector current with
A) Base current B) Reverse saturation current C) Emitter current D) VCC.

**(04 Marks)**

b. What is the meaning of transistor biasing? Draw a neat sketch to explain the base biasing of a transistor in CE mode. What is its stability factor S? **(08 Marks)**

c. Draw the DC load line for the voltage-divider biasing circuit shown in Fig.Q.3(c). Find the collector current and the Q point. **(08 Marks)**

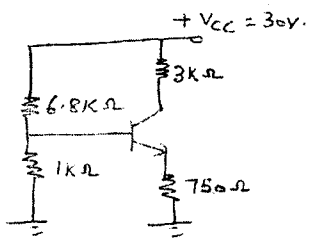



Fig.Q.3(c).

4 a. i) The SCR is a _____ device
A) NPN B) PNP C) PNPN D) PNN

ii) A relaxation oscillator uses
A) MOSFET B) SCR C) UJT D) BJT

iii) An FET is a _____ controlled device
A) Voltage B) Power C) Current D) Doping

iv) The gate current in a JFET is
A) Very large B) Very small C) Significant D) Depends on the input voltage.

**(04 Marks)**

b. Draw the structure and symbol of an SCR. Explain its operation and V-I characteristics. **(08 Marks)**

c. Explain the construction and working of an UJT. **(08 Marks)**

## PART – B

5 a. i) The stability of an amplifier_____ with negative feedback
A) Improves B) Deteriorates
C) is not affected D) Depends on amount of negative feedback

ii) The Barkhausen criterion states that
A) $A = B$ B) $A = \frac{1}{\beta}$ C) $A\beta = 1$ D) $A\beta = 0$.

iii) In an oscillator we use _____ feedback
A) Positive B) Negative C) Neither D) Unity gain

iv) The input capacitor in a CE amplifier blocks
A) AC signal B) DC component
C) Both AC and DC D) Noise of a particular frequency **(04 Marks)**

b. Draw a neat circuit diagram of Hartley's oscillator and explain its working. What is the frequency of oscillations? **(08 Marks)**

c. Design a Colpitt's oscillator for a frequency of oscillation of 100 kHz. **(08 Marks)**

6 a. i) The op amp is basically a _____ amplifier
A) Positive feedback B) Differential
C) Common emitter D) Common – signal

ii) In an inverting amplifier, $R_1$ = 1K and $R_f$ = 2K. If input voltage is 2V, output voltage is
A) –2V B) –0.5 V
C) 4V D) –4V

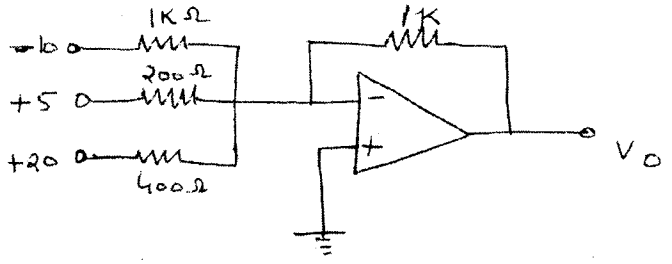
iii) The CMMR should be
A) Close to unity B) Much larger than unity
C) Zero D) Much smaller then unity

iv) When both the inputs of op amp are grounded, the voltage across the output is called
A) Output off set voltage B) Output grounded voltage
C) Output bias voltage D) Output common voltage **(04 Marks)**

b. What are characteristics of an ideal op amp? **(04 Marks)**

c. Show with a circuit diagram how the op amp can be used as an integrator. **(06 Marks)**

d. Find the output voltage for the circuit below. **(06 Marks)**




7 a. i) $(11011)_2 = (\_\_\_\_\_)_8$
A) $(33)_8$ B) $(17)_8$ C) $(25)_8$ D) $(28)_8$

ii) The 2'S complement of 1100110 is
A) 0011001 B) 0011010 C) 1100001 D) 1100010

iii) The BCD representation of decimal 10 is
A) 00001010 B) 00001001 C) 00010000 D) 10100000

iv) The binary of $(A5)_{16}$ is
A) 00100111 B) 00100101 C) 10100101 D) 10100011 **(04 Marks)**

b. Draw the block diagram of a super hetrodyne AM receiver and explain the function of each block. **(08 Marks)**

c. i) Convert $(10110011010)_2$ into octal, decimal and hexadecimal; ii) Subtract using 2'S complement $(15 - 7)_{10}$. **(08 Marks)**

8 a. i) A + AB = _____
A) AB B) A C) B D) 1 + A

ii) Universal gate is
A) NOT B) AND C) OR D) NAND

iii) If x + 1 = 1 and x . 1 = 0, then x is
A) 0 B) 1 C) Could be 0 or 1 D) Situation can never be true.

iv) The output is high only when both inputs are zero to a gate. The gate is
A) AND B) NOR C) OR D) NAND. **(04 Marks)**

b. Draw a full adder circuit with the truth table. **(06 Marks)**

c. Simplify $ABC + AB\overline{C} + \overline{A}BC$. **(04 Marks)**

d. Implement OR and AND gates using NOR gates. **(06 Marks)**



* * * * *

Srinivas Institute of Technology
Library, Mangalore

USN | | | | | | | | | | |

06ELN15/25

# First/Second Semester B.E. Degree Examination, Dec.09/Jan.10
# Basic Electronics

Time: 3 hrs. Max. Marks:100

**Note:** ***1. Answer any FIVE full questions, selecting at least TWO questions from each part.***
***2. Standard notations are used.***
***3. Missing data may be suitably assumed.***
***4. Answer all objective type questions only on OMR sheet, page 5 of answer book.***
***5. Objective type questions, if answered on other than OMR sheet, will not be valued.***

Important Note : 1. On completing your answers, comp ..orily draw diagonal cross lines on the remaining blank r..ges.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

## PART – A

1 a. i) The cut-in voltage of a Si-p-n diode is about.....
A) 0.6 V B) 0.6 mV C) 1.2 V D) 1.2 mV

ii) The ripple factor for a full-wave rectifier is.....
A) 0.482 B) 0.5 C) 1.21 D) -1.21

iii) The Zener resistance of a Zener diode, which exhibits 50 mV change in $V_z$ for a 2.5 mA change in $I_z$ is.....
A) 10 Ω B) 40 Ω C) 20 Ω

iv) The average output voltage of half wave rectifier with an input of 300 Sin 314t is .....
A) 100 V B) 95.49 V C) 90.49 V D) 90.0 V. **(04 Marks)**

b. Draw and explain the V-I characteristic of Si and Ge diodes. **(06 Marks)**

c. Draw the circuit of a half wave rectifier and explain its working with necessary waveforms. **(06 Marks)**

d. A diode with $V_F = 0.7$ V is connected as a half wave rectifier. The load resistance is 600 Ω and the (rms) ac input is 24V. Determine the peak output voltage, the peak load current and the diode peak reverse voltage. **(04 Marks)**

2 a. i) The doping of the emitter region of a transistor is ..... the base region.
A) Greater than B) Equal to C) Less than D) Much lesser than

ii) If $\alpha = 0.95$, then the value of $\beta$ of the transistor is .....
A) 190 B) 19 C) 0.05 D) 25

iii) The input resistance is highest for.....
A) CB amplifier B) CC amplifier C) CE amplifier D) None of these

iv) For cascading one should use.....
A) CE configuration B) CB configuration
C) CC configuration D) None of these. **(04 Marks)**

b. Draw a block diagram of an un-biased n-p-n transistor. Identify each part of the device and show the depletion regions and barrier voltages. Briefly explain. **(05 Marks)**

c. Write equations for collector current ($I_C$) in terms of emitter current ($I_E$) and $\alpha_{dc}$, and in terms of base current ($I_B$) and $\alpha_{dc}$. Define $\alpha_{dc}$ and $\beta_{dc}$ and mention typical values for each. **(05 Marks)**

d. For the circuit diagram shown in Fig.2(d), a Si transistor with $\beta = 50$ is used. Draw the d.c. load line and determine the operating point. **(06 Marks)**

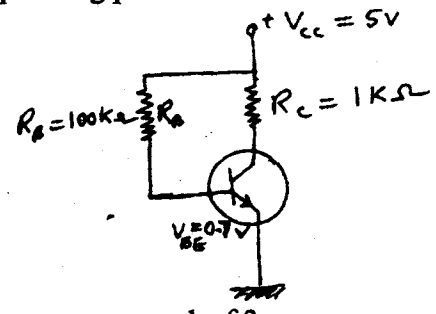



Fig.2(d).

3 a. i) For an emitter follower, the voltage gain is.....
A) Unity B) Greater than unity C) Less than unity D) Zero

ii) The self bias arrangement gives a better Q point stability when.....
A) Re is small B) β is small but Re is large
C) Both β and Re are large D) None of these

iii) The load line moves parallel to itself on the CE output characteristics of a transistor when.....
A) $R_L$ changes B) $V_{CC}$ changes
C) Both $R_L$ and $V_{CC}$ change D) None of these

iv) To work as a linear amplifier a transistor must operate in....
A) Active region B) Saturation region
C) Nonlinear region D) Cut-off region. **(04 Marks)**

b. Compare base bias, collector to base bias and voltage divider bias with regard to stability of the transistor collector voltage with spread in $h_{FE}$ value. **(10 Marks)**

c. Design a collector to base bias circuit shown in Fig.3(c) with the following specifications $V_{CE} = 5$ V, $I_C = 5$ mA, $V_{CC} = 15$ V and $h_{FE} = 100$, $V_{BE} = 0.7$ V. **(06 Marks)**

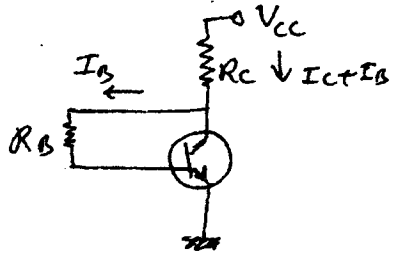



Fig.3(c).

4 a. i) The FET is a ..... controlled device
A) Current B) Voltage C) Power D) None of these

ii) Which of the following devices is expected to have the highest input impedance...?
A) MOSFET B) BJT C) JFET

iii) The SCR is used as a.....
A) Ordinary rectifier B) Controlled rectifier
C) Amplifier D) None of these

iv) An initial saturated drain current can be attained in an n-channel JFET when $V_{GS}$ is equal to.....
A) Pinch off voltage B) zero volts C) – 4 V. **(04 Marks)**

b. Draw a circuit diagram to obtain the drain characteristics for an n-channel JFET. Thus draw drain characteristics and explain them. **(08 Marks)**

c. Sketch typical SCR forward and reverse characteristics. Identify all regions of characteristics and all important current and voltage levels. **(08 Marks)**

## PART – B

5 a. i) An audio amplifier works over the frequency range.....
A) 20 Hz to 20 kHz B) 20 Hz to 1 MHz C) 1 kHz to 4 kHz

ii) An oscillator requires ..... feed back for its operations
A) Negative B) Positive C) High D) Low

iii) The frequency of a Hartley oscillator for $L_1 = L_2 = 50$ mH and C = 200 pF is.....
A) 50.3 kHz B) 100 kHz C) 150 kHz

iv) The conditions Aβ = 1 for oscillations is known as the ..... criterion
A) Nyquist's B) Barkhaular
C) Routh – Horwitz D) None of these. **(04 Marks)**

b. With a neat circuit diagram, explain the working of single stage RC coupled amplifier, and thus draw frequency response curve and explain the curve. **(10 Marks)**

c. List and explain the advantages of negative feedback in amplifiers. **(06 Marks)**

6 a. i) The CMRR of an OP-AMP is.....
A) Greater than 1 B) Less than 1 C) Equal to 1

ii) The OP-AMP 741 has an open loop voltage gain of.....
A) $2 \times 10^5$ B) $2 \times 10^{-5}$ C) $3 \times 10^{10}$

iii) The inverting amplifier circuit has an input resistance $R_1$ = 1 KΩ, feed back resistance $R_F$ = 3 KΩ. The output voltage is....
A) 6 V B) 12 V C) 18 V

iv) Lissajous figures are used to measure..... difference between two sinusoidal signals
A) Phase B) Amplitude C) Frequency. **(04 Marks)**

b. What are the ideal characteristics of OP – AMP? **(04 Marks)**

c. With a neat diagram, explain the working of an op-amp as summing amplifier. **(06 Marks)**

d. Show how op-amp can be used as an inverting amplifier. Derive an expression for the voltage gain. **(06 Marks)**

7 a. i) The AM signal that occupies the greatest bandwidths is the one modulated by....
A) 1 kHz sine wave B) 10 kHz sine wave
C) 1 kHz square wave D) 5 kHz square wave

ii) The circuit that recovers the original modulating information from an AM signal is known as.....
A) Modulator B) Mixer
C) Demodulator D) Oscillator

iii) On an FM signal, maximum deviation occurs at .....
A) Zero crossing point B) Peak positive amplitude
C) Peak negative amplitude D) Both (A) and (B)

iv) The binary equivalent of the decimal member 5 is....
A) 100 B) 101
C) 110 D) 1001. **(04 Marks)**

b. Explain with neat wave forms the principle of amplitude modulation. Write the expression for AM wave. **(06 Marks)**

c. A 500 W, 100 kHz carrier is modulated to a depth of 60 % by modulating signal frequency of 1 kHz. Calculate the total power transmitted. What are the sideband components of the AM wave? **(05 Marks)**

d. Convert the following binary numbers to decimal numbers.
i) 1101 ii) 10001 iii) 10101. **(05 Marks)**

8 a. i) The Boolean expression Y = A.B represents....
A) OR gate B) XNOR gate
C) AND gate D) NOT gate

ii) To add two m-bit number, the number of required half adders is.....
A) 2 m-1 B) 2 m
C) $2^m$-1 D) 2m + 1

iii) The decimal number 37 is represented in BCD by .....
A) 100111 B) 00111011
C) 00110111 D) 111100

iv) A NOT circuit can be built by using.....
A) MOSFET B) Diode
C) Zener diode D) BJT. **(04 Marks)**

b. Write the truth table of an OR function and realize an OR gate using diodes. **(05 Marks)**

c. Simplify and realize the following using NAND gates $A\ \overline{B}\ \overline{C} + \overline{A}\ \overline{B}\ \overline{C} + \overline{A}\ \overline{B} + \overline{A}\ \overline{C}$. **(05 Marks)**

d. Realize a half adder using AND, OR and inverter logic gates. Write the truth table. **(06 Marks)**

* * * * *

Srinivas Institute of Technology
Library, Mangalore

USN | | | | | | | | | | |

06ELN15/25

# First/Second Semester B.E. Degree Examination, May/June 2010
## Basic Electronics

Time: 3 hrs. Max. Marks:100

**Note:** *1. Answer any FIVE full questions, choosing at least two questions from each part.*
*2. Answer all objective type questions only on OMR sheet page 5 of the answer booklet.*
*3. Answer to objective type questions on sheets other than OMR will not be valued.*

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

### PART – A

1 a. Choose the correct answer from the following :
i) Semiconductor materials have _____ bonds.
A) Covalent B) Mutual C) Metalic D) Ionic.
ii) Junction breakdown occurs with
A) Forward bias B) Reverse bias C) Active bias D) under high temperature.
iii) In a silicon diode, reverse current is usually
A) Zero B) Very large C) Very small D) In the breakdown region.
iv) In a Zener diode
A) Forward voltage rating is high
B) Negative resistance characteristic exists
C) Sharp breakdown occurs at low reverse voltage
D) None of the above. **(04 Marks)**

b. With diagram and waveform, explain the working principle of full wave rectifier. **(08 Marks)**

c. A half wave rectifier is used to convert 230 V AC in to DC across a load of 1 k Ω. The transformer used is 230 V/12 volts. The DC resistance of the transformer used is 12Ω and the resistance of the diode is 22 Ω. Compute :
i) DC output voltage
ii) The rms value of the output voltage
iii) Ripple factor
iv) Rectification efficiency. **(08 Marks)**

2 a. Choose the correct answer from the following :
i) The DC – Loadline of a transistor circuit
A) Is a curved line B) Has a–ve slope
C) Does not contain Q point D) Gives graphical relation between $I_C$ and $I_B$.
ii) The correct relationship between α and β is.
A) $\beta = \frac{\alpha}{1-\alpha}$ B) $\alpha = \frac{\beta}{1+\beta}$ C) $\alpha = \frac{\beta}{1-\beta}$ D) $1-\alpha = \frac{1}{1+\beta}$.
iii) In the base region of p-n-p transistor, the main stream of current is
A) Hole current B) Electron current C) Saturation current D) Breakdown current.
iv) The transistor operating point is chosen along the
A) X-axis B) Load line C) Resistance line D) Characteristic.
**(04 Marks)**

b. Draw the current components which flow in a transistor. Also derive the equation for $I_c$ in terms of $\alpha_{dc}$, $I_{CBO}$ and $I_B$. **(08 Marks)**

c. Draw the input and output characteristics of CE circuit. Explain active, saturation and cut off regions. **(08 Marks)**

3 a. Choose the correct answer from the following :

i) A transistor is a

A) Two terminal device B) Reverse biased device

C) Three terminal device D) Modulated device.

ii) Biasing means

A) Heating the junction B) Applying voltages C) Discharging D) Destroying.

iii) Stability factor for a fixed bias circuit is

A) $1 + \alpha$ B) $1 - \alpha$ C) $1 + \beta$ D) $1 - \beta$.

iv) The operating point must be ___ for proper operation of the transistor

A) High B) Increasing C) Stable D) Decreasing.

**(04 Marks)**

b. Give the circuit for i) Collector to base bias ii) emitter current bias. Also compare basic bias circuits. **(08 Marks)**

c. For the circuit shown in Fig. Q3(c) using Si transistor with $\beta = 50$, draw the d.c loadline and determine the operating point. **(08 Marks)**

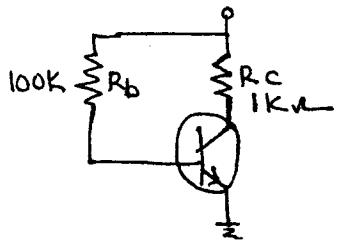



Fig. Q3(c)

4 a. Choose the correct answer from the following :

i) The situation of drain current becoming just saturated is called

A) Forward bias B) Saturation C) Pinch off D) Cutoff.

ii) An SCR is a ____ device

A) Amplifying B) Switching C) Negative D) Blocking.

iii) The minimum point in VI characteristic of UJT is known as ___ point

A) Negative B) Valley C) Latching D) Conducting.

iv) The factor $\eta$ of UJT is known as ____ ratio.

A) ON B) Pulse C) Negative D) Intrinsic stand–off.

**(04 Marks)**

b. With the help of equivalent circuit and characteristics, explain the working principle of UJT. **(08 Marks)**

c. Draw two transistor equivalent circuit of SCR. Also plot V-I characteristic and explain various regions of operation. **(08 Marks)**

## PART - B

5 a. Choose the correct answer from the following :

i) The criteria for producing Oscillations are known as ___ criteria.

A) Doppler B) Bark housen C) Miller D) Band width.

ii) A quartz crystal may be represented by an equivalent circuit consisting of a series ___ circuit.

A) RC B) LC C) RLC D) RL.

iii) The oscillating circuit is also called as

A) Differential B) Tank C) Logic D) CRT.

iv) Unit of gain in logarithmic scale is called

A) Watt B) Joul C) Bel D) Decibel. **(04 Marks)**

b. With circuit, explain the working of BJT RC phase shift oscillator. **(08 Marks)**

c. With circuit, explain the working of two stage RC coupled amplifier and draw its frequency response. **(08 Marks)**

6 a. Choose the correct answer from the following :

i) An inverting amplifier is one that produces ____ phase shift between its input and output voltage.

A) 45° B) 90° C) 360° D) 180°.

ii) An op-amp shorted between inverting terminal and output terminal is called

A) Adder B) Integrator C) Voltage-follower D) inverter.

iii) The op-amp can amplify

A) AC signals only B) DC signals only C) both AC and DC signals D) None of these.

iv) The op-amp integrator uses

A) Inductors B) Miller effect C) Sinusoidal inputs D) Hysteresis. **(04 Marks)**

b. Draw the circuit, using op-amp, for

i) Integrator ii) Differentiator iii) Adder iv) Voltage follower. **(08 Marks)**

c. With diagram, explain main parts of CRT. **(08 Marks)**

7 a. Choose the correct answer from the following :

i) The 1's complement of 1010 gives

A) 1111 B) 0001 C) 0010 D) 1110.

ii) The number 12 in octal is equivalent to decimal

A) 20 B) 12 C) 10 D) 4.

iii) In binary numbers, shifting the binary point one place to the right

A) Devides by 2 B) decreases by 10 C) Increases by 10 D) Multiplies by 2.

iv) To represent 35 in binary, number of bits required is

A) 6 B) 5 C) 4 D) 33. **(04 Marks)**

b. Explain the need for modulation. **(08 Marks)**

c. perform the following :

i) $240_{10} =$ _____$_2$

ii) $0.2315_{10} =$ _____$_2$

iii) $3312_8 =$ _____$_2$

iv) $32198_{10} =$ _____$_{BCD}$. **(08 Marks)**

8 a. Choose the correct answer from the following :

i) The expression for half adder carry C with inputs A and B is given by

A) A + B B) AB C) $\overline{A}\,\overline{B}$ D) None of these.

ii) A + AB =

A) AB B) A C) B D) 1 + A.

iii) universal gates are _____ and _____

A) NOT and NOR B) AND and OR C) NAND and NOR D) EXOR and EXNOR.

iv) A + AB + A =

A) AB B) A + B C) A D) O. **(04 Marks)**

b. i) Implement Y=ABCD using two input NAND gates

ii) Simplify $Y = (A + B)\left(\overline{A} + C\right)\left(\overline{B} + C\right)$. **(08 Marks)**

c. With a circuit, explain the working principle of parallel binary adder. **(08 Marks)**

* * * * *